

# DATA SHEET

**74LV4094**

8-stage shift-and-store bus register

Product specification

1998 Jun 23

## 8-stage shift-and-store bus register

## 74LV4094

## FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25^{\circ}\text{C}$
- Output capability: standard
- $I_{CC}$  category: MSI

## Applications:

- Serial-to-parallel data conversion
- Remote control holding register

## DESCRIPTION

The 74LV4094 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT4094.

The 74LV4094 is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input (D) to the parallel buffered 3-State outputs (QP<sub>0</sub> to OP<sub>7</sub>). The parallel outputs may be connected directly to the common bus lines. Data is shifted on the positive-going clock (CP) transitions. The data in each shift register is transferred to the storage register when the strobe input (STR) is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) signal is HIGH. Two serial outputs (QS<sub>1</sub> and QS<sub>2</sub>) are available for cascading a number of 74LV4094 devices. Data is available at QS<sub>1</sub> on the positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at QS<sub>2</sub> on the next negative going clock edge and is for cascading 74LV4094 devices when the clock rise time is slow.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay CP to QS <sub>1</sub> CP to QS <sub>2</sub> CP to QP <sub>n</sub> STR to QP <sub>n</sub>	$C_L = 15$ pF; $V_{CC} = 3.3$ V	14	ns
			13	
			18	
			17	
$f_{MAX}$	Maximum clock frequency		95	MHz
$C_I$	Input capacitance		3.5	pF
$C_{PD}$	Power dissipation capacitance per gate	$V_{CC} = 3.3$ V $V_I = \text{GND to } V_{CC}$ NO TAG	83	pF

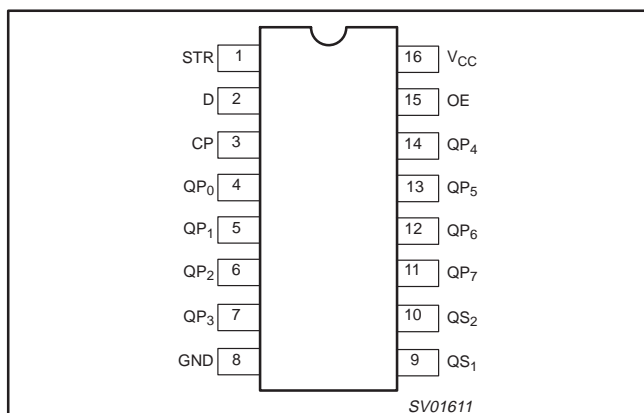
## NOTE:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	-40°C to +125°C	74LV4094 N	74LV4094 N	SOT38-4
16-Pin Plastic SO	-40°C to +125°C	74LV4094 D	74LV4094 D	SOT109-1

## PIN CONFIGURATION



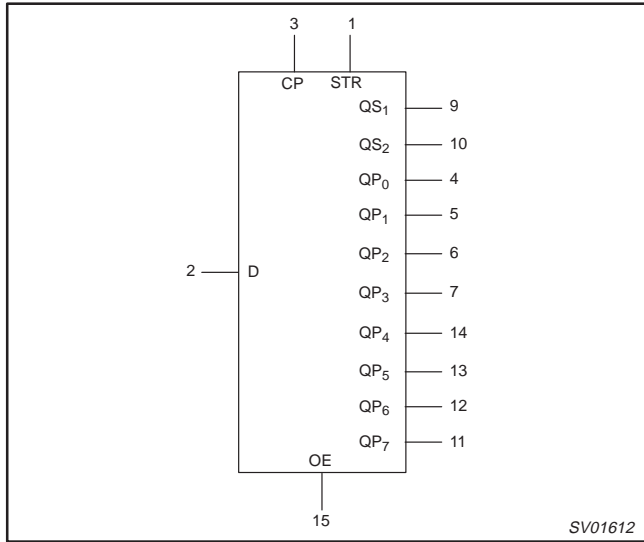
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	STR	Strobe input
2	D	Serial input
3	CP	Clock input
4, 5, 6, 7, 14, 13, 12, 11	QP <sub>0</sub> to QP <sub>7</sub>	Parallel outputs
8	GND	Ground (0 V)
9, 10	QS <sub>1</sub> , QS <sub>2</sub>	Serial outputs
15	OE	Output enable input
16	$V_{CC}$	Positive supply voltage

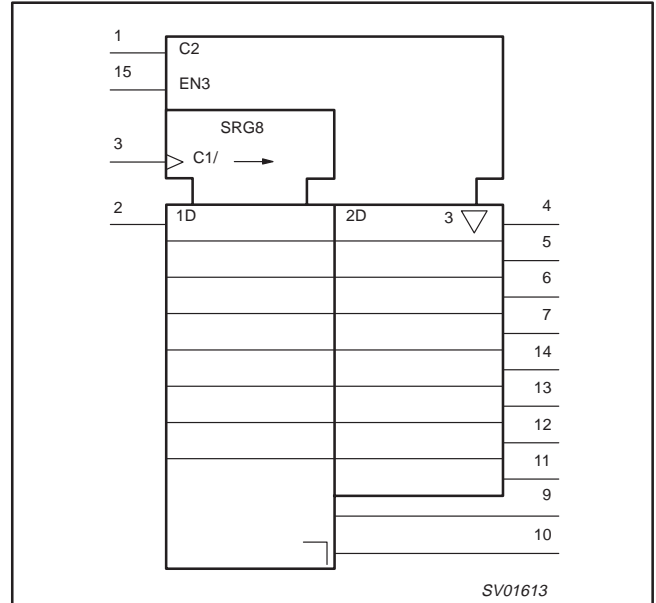
# 8-stage shift-and-store bus register

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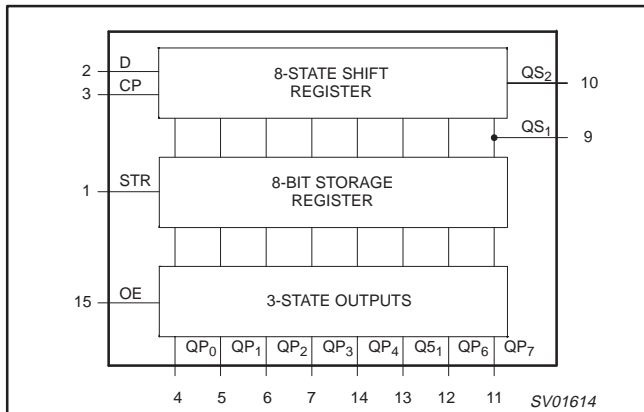
## LOGIC SYMBOL



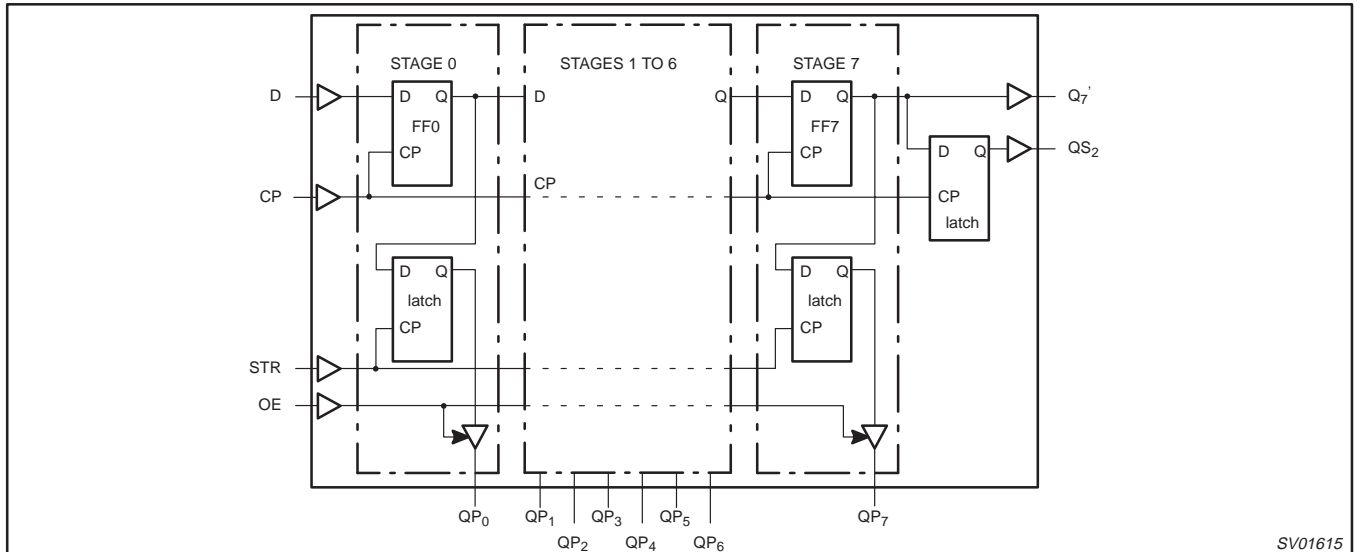
## LOGIC SYMBOL (IEEE/IEC)



## FUNCTIONAL DIAGRAM



## LOGIC DIAGRAM



# 8-stage shift-and-store bus register

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## FUNCTION TABLE

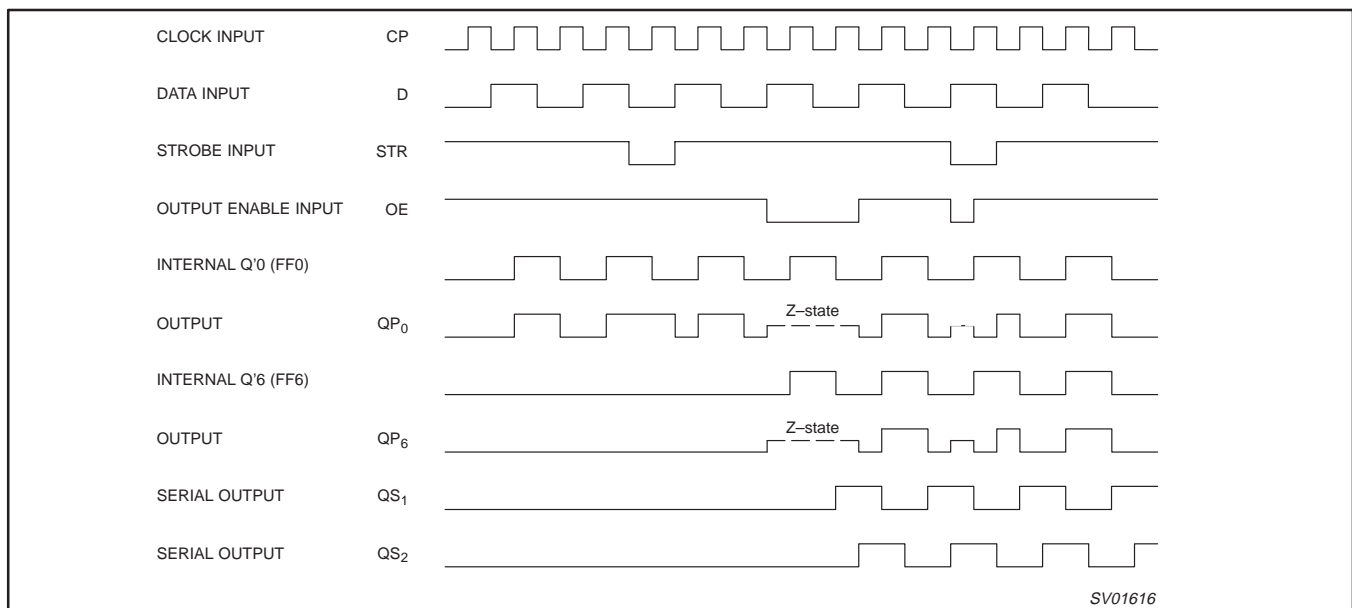
INPUTS				PARALLEL OUTPUT		SERIAL OUTPUTS	
CP	OE	STR	D	QP <sub>0</sub>	QP <sub>n</sub>	QS <sub>1</sub>	QS <sub>2</sub>
↑	L	X	X	Z	Z	Q' <sub>6</sub>	NC
↓	L	X	X	Z	Z	NC	QP <sub>7</sub>
↑	H	L	X	NC	NC	Q' <sub>6</sub>	NC
↑	H	H	L	L	QP <sub>n-1</sub>	Q' <sub>6</sub>	NC
↑	H	H	H	H	QP <sub>n-1</sub>	Q' <sub>6</sub>	NC
↓	H	H	H	NC	NC	NC	QP <sub>7</sub>

**NOTES:**

- H = HIGH voltage level
- L = LOW voltage level
- X = don't care
- Z = high impedance OFF-state
- NC = no change

- ↑ = LOW-to-HIGH CP transition
- ↓ = HIGH-to-LOW CP transition
- Q'<sub>6</sub> = the information in the 8<sup>th</sup> register stage is transferred to the 8<sup>th</sup> register stage and QS<sub>n</sub> clock edge.

## TIMING DIAGRAM



## 8-stage shift-and-store bus register

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**ABSOLUTE MAXIMUM RATINGS** NO TAG, NO TAG

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND},$ $\pm I_{CC}$	DC $V_{CC}$ or GND current for types with – standard outputs		50	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: -40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC}$	DC supply voltage	See Note NO TAG	1.0	3.3	3.6	V
$V_I$	Input voltage		0	–	$V_{CC}$	V
$V_O$	Output voltage		0	–	$V_{CC}$	V
$T_{amb}$	Operating ambient temperature range in free air	See DC and AC characteristics	-40 -40		+85 +125	°C
$t_r, t_f$	Input rise and fall times except for Schmitt-trigger inputs	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$	– – –	– – –	500 200 100	ns/V

**NOTE:**

- The LV is guaranteed to function down to  $V_{CC} = 1.0V$  (input levels GND or  $V_{CC}$ ); DC characteristics are guaranteed from  $V_{CC} = 1.2V$  to  $V_{CC} = 5.5V$ .

## 8-stage shift-and-store bus register

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**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP NO TAG	MAX	MIN	MAX	
$V_{IH}$	HIGH level Input voltage	$V_{CC} = 1.2\text{ V}$	$V_{CC}$	0.6		$V_{CC}$		V
		$V_{CC} = 2.0\text{ V}$	1.4			1.4		
		$V_{CC} = 2.7\text{ to }3.6\text{ V}$	2.0			2.0		
$V_{IL}$	LOW level Input voltage	$V_{CC} = 1.2\text{ V}$		0.4	GND		GND	V
		$V_{CC} = 2.0\text{ V}$			0.6		0.6	
		$V_{CC} = 2.7\text{ to }3.6\text{ V}$			0.8		0.8	
$V_{OH}$	HIGH level output voltage; all outputs	$V_{CC} = 1.2\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; -I_O = 100\mu\text{A}$		1.2				V
		$V_{CC} = 2.0\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; -I_O = 100\mu\text{A}$	1.8	2.0		1.8		
		$V_{CC} = 2.7\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; -I_O = 100\mu\text{A}$	2.5	2.7		2.5		
		$V_{CC} = 3.0\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; -I_O = 100\mu\text{A}$	2.8	3.0		2.8		
$V_{OH}$	HIGH level output voltage; STANDARD outputs	$V_{CC} = 3.0\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; -I_O = 6\text{mA}$	2.40	2.82		2.20		V
$V_{OL}$	LOW level output voltage; all outputs	$V_{CC} = 1.2\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; I_O = 100\mu\text{A}$		0				V
		$V_{CC} = 2.0\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; I_O = 100\mu\text{A}$		0	0.2		0.2	
		$V_{CC} = 2.7\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; I_O = 100\mu\text{A}$		0	0.2		0.2	
		$V_{CC} = 3.0\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; I_O = 100\mu\text{A}$		0	0.2		0.2	
$V_{OL}$	LOW level output voltage; STANDARD outputs	$V_{CC} = 3.0\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; I_O = 6\text{mA}$		0.25	0.40		0.50	V
$I_I$	Input leakage current	$V_{CC} = 3.6\text{ V}; V_I = V_{CC}\text{ or GND}$			1.0		1.0	$\mu\text{A}$
$I_{OZ}$	3-State output OFF-state current	$V_{CC} = 3.6\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; V_O = V_{CC}\text{ or GND}$			5		10	$\mu\text{A}$
$I_{CC}$	Quiescent supply current; SSI	$V_{CC} = 3.6; V_I = V_{CC}\text{ or GND}; I_O = 0$			20.0		40	$\mu\text{A}$
$I_{CC}$	Quiescent supply current; flip-flops	$V_{CC} = 3.6; V_I = V_{CC}\text{ or GND}; I_O = 0$			20.0		80	$\mu\text{A}$
	Quiescent supply current; MSI	$V_{CC} = 3.6\text{ V}; V_I = V_{CC}\text{ or GND}; I_O = 0$			20.0		160	$\mu\text{A}$
	Quiescent supply current; LSI	$V_{CC} = 3.6\text{ V}; V_I = V_{CC}\text{ or GND}; I_O = 0$			500		1000	
$\Delta I_{CC}$	Additional quiescent supply current per input	$V_{CC} = 2.7\text{ V to }3.6\text{ V}; V_I = V_{CC} - 0.6\text{ V}$			500		850	$\mu\text{A}$

**NOTE:**

1. All typical values are measured at  $T_{amb} = 25^\circ\text{C}$ .

# 8-stage shift-and-store bus register

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## AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.5\text{ns}$ ;  $C_L = 50\text{pF}$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				-40 to +85 °C			-40 to +125 °C		
				$V_{CC}$ (V)	MIN	TYP <sup>1</sup>	MAX	MIN	
$t_{PHL}/t_{PLH}$	Propagation delay CP to QS <sub>1</sub>		1.2		90				ns
			2.0		31	58		70	
			2.7		23	43		51	
			3.0 to 3.6		17 <sup>2</sup>	34		41	
$t_{PHL}/t_{PLH}$	Propagation delay CP to QS <sub>2</sub>		1.2		80				ns
			2.0		27	51		61	
			2.7		20	38		45	
			3.0 to 3.6		14 <sup>2</sup>	30		36	
$t_{PHL}/t_{PLH}$	Propagation delay CP to QP <sub>n</sub>		1.2		115				ns
			2.0		39	75		90	
			2.7		29	55		66	
			3.0 to 3.6		22 <sup>2</sup>	44		53	
$t_{PHL}/t_{PLH}$	Propagation delay STR to QP <sub>n</sub>		1.2		105				ns
			2.0		36	68		82	
			2.7		26	50		60	
			3.0 to 3.6		20 <sup>2</sup>	40		48	
$t_{PZH}/t_{PZL}$	3-State Output enable time OE to QP <sub>n</sub>		1.2		100				ns
			2.0		34	65		77	
			2.7		25	48		56	
			3.0 to 3.6		19 <sup>2</sup>	38		45	
$t_{PHZ}/t_{PLZ}$	3-State Output disable time OE to QP <sub>n</sub>		1.2		65				ns
			2.0		24	40		49	
			2.7		18	32		37	
			3.0 to 3.6		14 <sup>2</sup>	26		30	
$t_w$	Clock pulse width HIGH or LOW		2.0	34	9		41		ns
			2.7	25	6		30		
			3.0 to 3.6	20	5 <sup>2</sup>		24		
$t_w$	Strobe pulse width; HIGH		2.0	34	9		41		ns
			2.7	25	6		30		
			3.0 to 3.6	20	5 <sup>2</sup>		24		
$t_{su}$	Set-up time D to CP		1.2		25				ns
			2.0	22	9		26		
			2.7	16	6		19		
			3.0 to 3.6	13	5 <sup>2</sup>		15		
$t_{su}$	Set-up time CP to STR		1.2		50				ns
			2.0	43	17		51		
			2.7	31	13		38		
			3.0 to 3.6	25	10 NO TAG		30		

# 8-stage shift-and-store bus register

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SYMBOL	PARAMETER	WAVEFORM	CONDITION						UNIT
			$V_{CC}$ (V)	-40 to +85 °C			-40 to +125 °C		
				MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$T_h$	Hold time D to CP		1.2		-10				ns
			2.0	5	-4		5		
			2.7	5	-3		5		
			3.0 to 3.6	5	-2 NO TAG		5		

**NOTES:**

1. Unless otherwise stated, all typical values are measured at  $T_{amb} = 25^{\circ}C$
2. Typical values are measured at  $V_{CC} = 3.3 V$ .



# 8-stage shift-and-store bus register

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## AC CHARACTERISTICS (Continued)

GND = 0 V;  $t_r = t_f \leq 2.5\text{ns}$ ;  $C_L = 50\text{pF}$

SYMBOL	PARAMETER	WAVEFORM	CONDITION		-40 to +85 °C			-40 to +125 °C		UNIT
			$V_{CC}$ (V)		MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$T_h$	Hold time D to STR		1.2			-25				ns
			2.0	5		-9		5		
			2.7	5		-6		5		
			3.0 to 3.6	5		-5 <sup>2</sup>		5		
$f_{max}$	Maximum clock pulse frequency		2.0	14	52		12		MHz	
			2.7	19	70		16			
			3.0 to 3.6	24	87 <sup>2</sup>		20			

**NOTES:**

1. Unless otherwise stated, all typical values are measured at  $T_{amb} = 25^\circ\text{C}$
2. Typical values are measured at  $V_{CC} = 3.3\text{ V}$ .

## AC WAVEFORMS

$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$

$V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ .

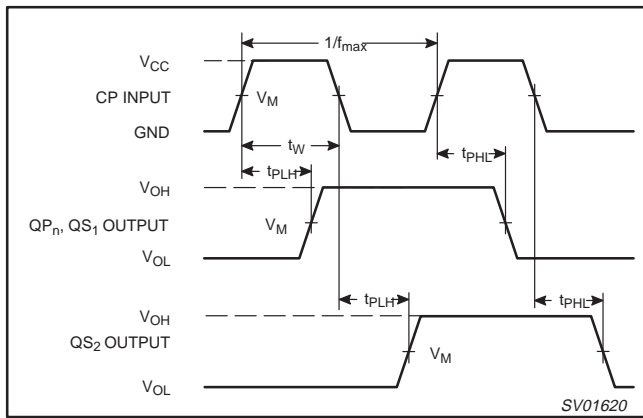
$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

$V_X = V_{OL} + 0.3\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$

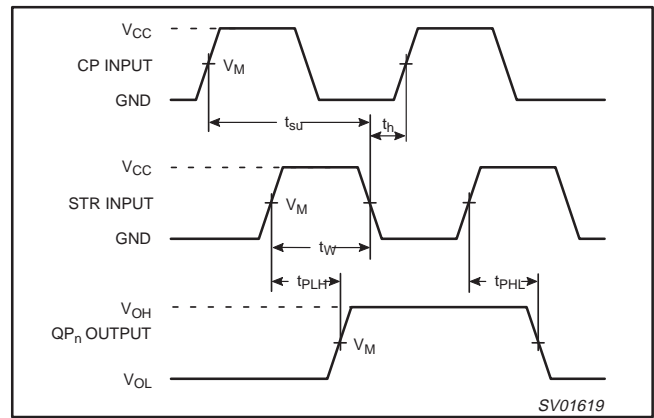
$V_X = V_{OL} + 0.1 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$

$V_Y = V_{OH} \pm 0.3\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$

$V_Y = V_{OH} \pm 0.1 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$



**Figure 1. Clock (CP) to output (QP<sub>n</sub>, QS<sub>1</sub>, QS<sub>2</sub>) propagation delays, the clock pulse width and the maximum clock frequency.**



**Figure 2. Strobe (STR) to output (QP<sub>n</sub>) propagation delays and the strobe pulse width and the clock set-up and hold times for strobe input.**

# 8-stage shift-and-store bus register

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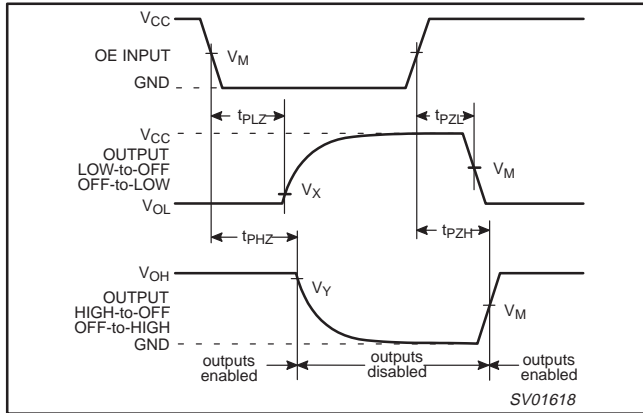


Figure 3. 3-State enable and disable times for input OE.

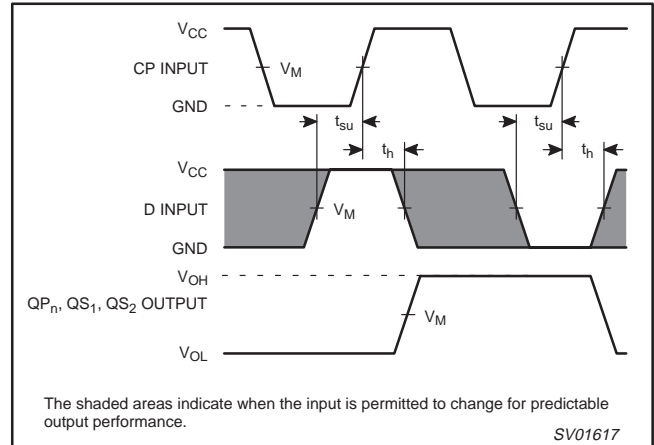


Figure 4. Data set-up and hold times for the data input (D).

## TEST CIRCUIT

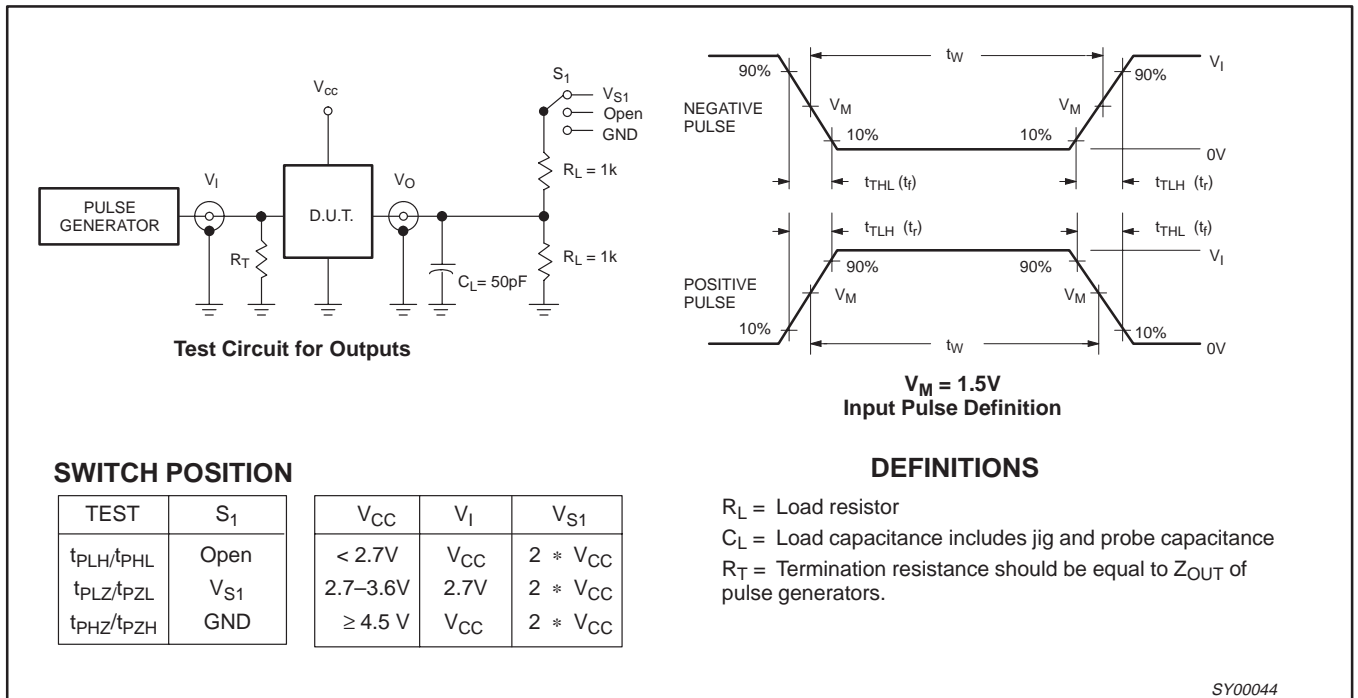


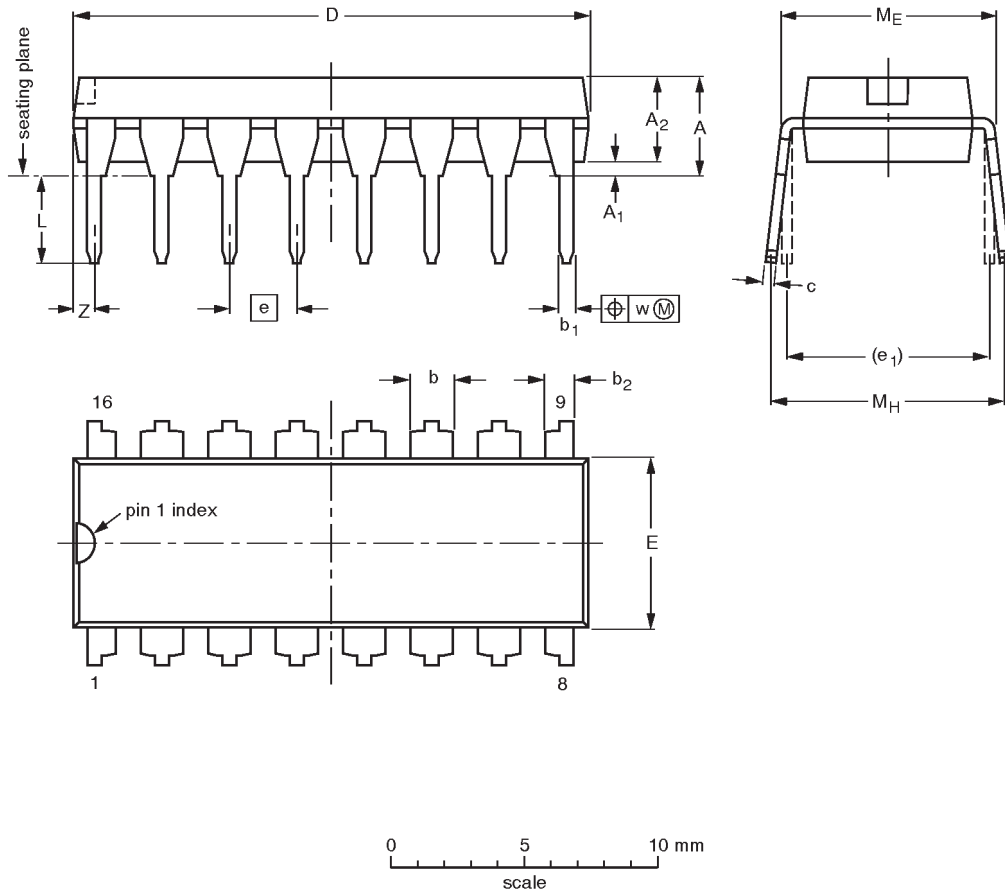
Figure 5. Load circuitry for switching times.

# 8-stage shift-and-store bus register

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

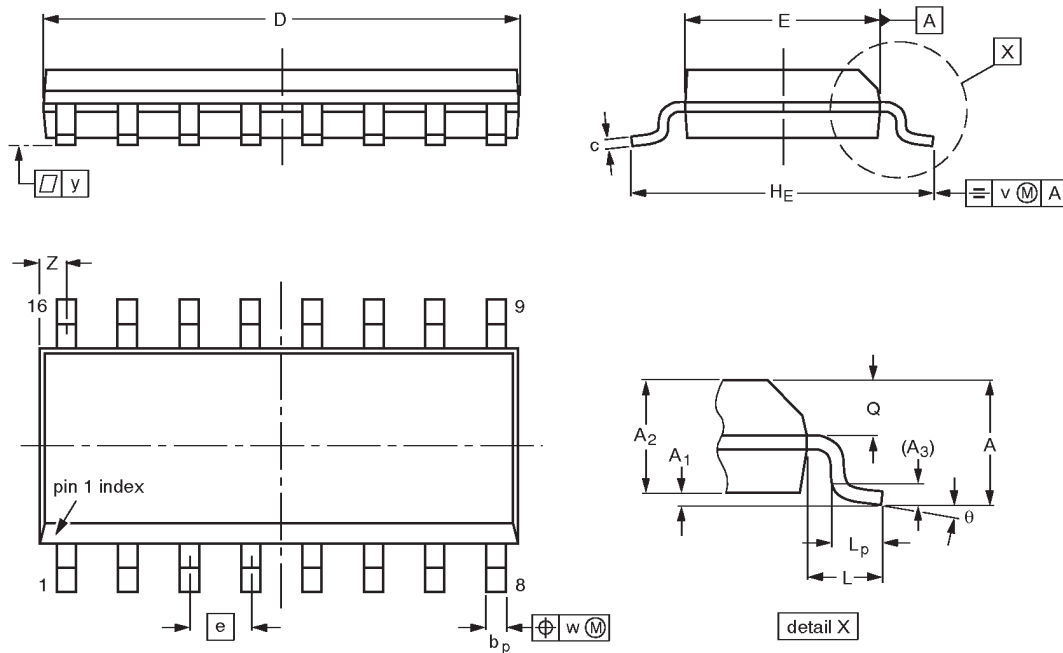
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

# 8-stage shift-and-store bus register

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**SO16: plastic small outline package; 16 leads; body width 3.9 mm**

**SOT109-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				91-08-13 95-01-23

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**NOTES**

## 8-stage shift-and-store bus register

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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